Journal of Advanced Engineering Research
ISSN: 2393-8447
Volume 11, Issue 1, 2024, pp.37-41

Design of an Electronically Tunable CMOS Band Pass Filter

Manish Rai[1,*], Raj Senani[1], Abdhesh Kumar Singh[2]
[1]Department of Electronics and Communication Engineering, NSUT (Main Campus), New Delhi-110078, India
[2] Department of Electronics and Communication Engineering, NSUT (East Campus), New Delhi-110031, India
*Corresponding author email: manish.rai.ec19@nsut.ac.in

ABSTRACT

This paper presents a CMOS band pass filter (BPF) design having provisions for independent electronic control of center frequency and bandwidth both. The topology is based upon the employment of two current feedback operational amplifiers which are currently finding favor of analog designers as an alternative to the classical voltage mode op-amps because of several advantages ofered by them. A CMOS voltage controlled floating resistance circuit is the other key element which has been employed to replace the center-frequency-controlling and bandwidth-controlling resistors in the considered configuration. The usefulness of the proposed design has been varified by the simulations on CADENCE SPICE by implementing the complete circuit using a CMOS CFOA alongwith the CMOS VCRs with 0.18µm CMOS technology parameters. Simulation results are given to estabilish the viability of the proposed design.

Keywords - Band pass filters, CMOS Circuits, CFOA, Voltage-controlled floating resistance, MOSFETs,

1. INTRODUCTION

Analog filters with electronically tunable parameters such as cutoff frequency/center frequency, bandwidth/ Q-factor and maximum gain are often required in many applications and a number of ways are known for realizing them using OTA-C or GM-C [1]-[7] techniques of realizing such filters which make use of electronically controllable OTAs or transconductors and usually do not employ external resistors. Some other techniques make use of analog multipliers in conjunction with standard biquads filters to obtain electronic control of filter parameter, such as [8]. In yet another technique, the designers employ electronically-controlled building blocks such as current controlled current conveyors [9] to realize such filters [10].

OTA-C based electronically controllable filters can provide linear control of various parameters through the external bias currents of the various OTAs but this advantage is available only when OTAs employed are BJT OTAs. In CMOS OTAs, their Gm is proportional to square root of the bias current (I_b) therefore, the linear control of parameters would not be available. On the other hand, the second-generation current controlled conveyer (CCCII) based filters [10] also provide linear control when CCII are implemented using bipolar architecture with CMOS CCCIIs the filter parameter control would be coming from g_ms which are proportional to square root of I_b. Thirdly, the multiplier-based filters can provide linear control of parameters but would require the incorporation of three to four analog multipliers, where external control voltages must be applied to get electronic control of filter parameters [10]. In comparison, the proposed configuration employs only two CMOS CFOAs along with the grounded capacitors, the grounded capacitors are suitable for integrated circuit (IC) and the circuit provides individualistic linear control of both bandwidth and center frequency through two different sets of control voltages. Moreover, the CMOS CFOAs, the CMOS floating VCR and the entire filter configuration all operate at very low power supply voltage of the order of ±1.5V. The usefulness of the designs are illustrated by CADENCE SPICE simulation results with the help of 0.18µm TSMC CMOS parameters.

2. PROPOSED CMOS BAND PASS FILTER DESIGN

The new electronically-controlled floating positive resistance circut [11] is shown in Fig.1. In this circuit, all the PMOS as well as NMOS MOSFETs are operating in saturation region and the circuit is free from body effects. To make easy of IC implementation, the body of all the PMOS transistors are connected with the highest positive level of supply (V_{dd}) and the body of all NMOS transistors to the highest negative level of the supply

(V_{ss}). Using mathematical analysis the relationship between the two-port voltages and corresponding currents of the floating resistance are given as:

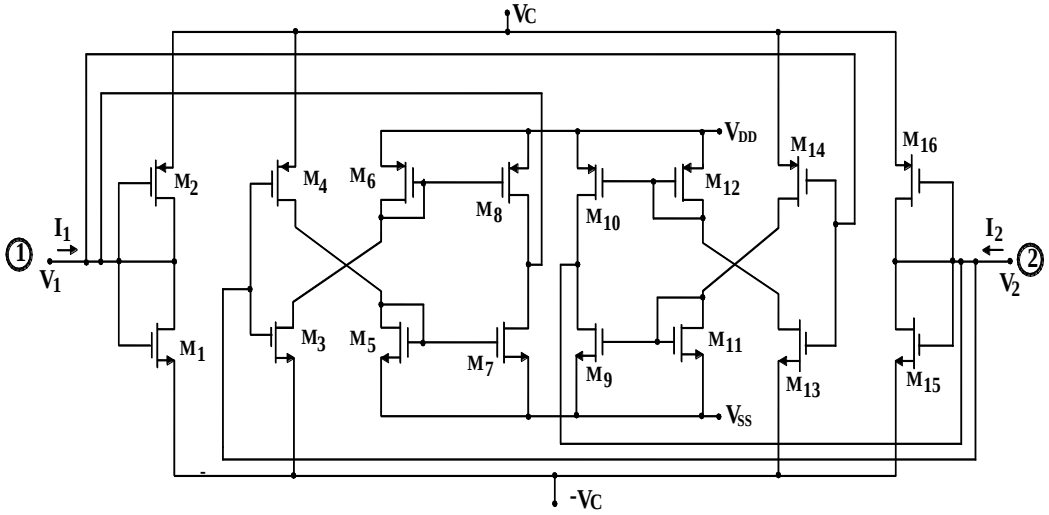
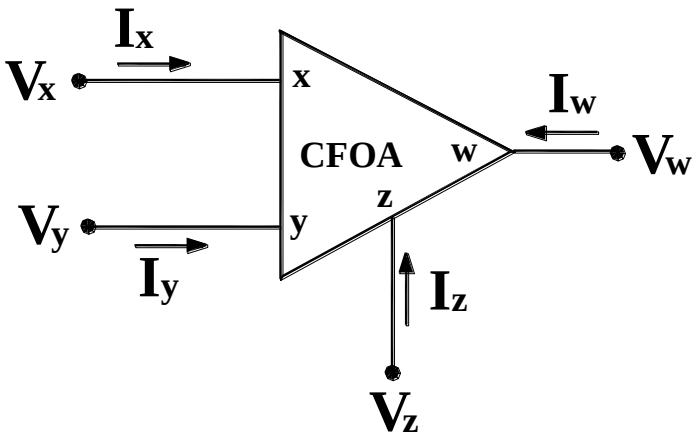
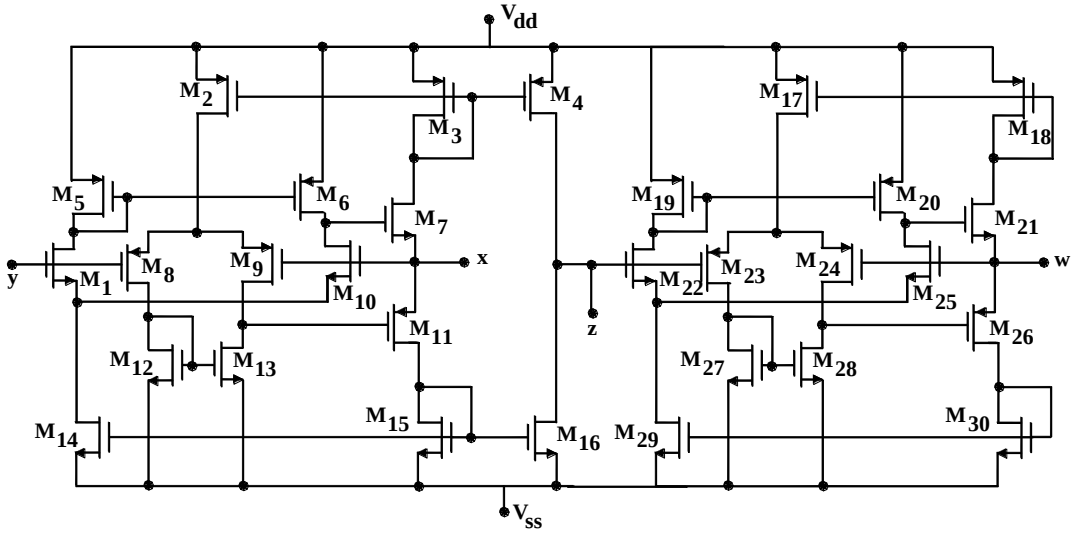


Fig.1 Floating voltage-controlled positive resistance (VCFPR) circuit



(a)



(b)

Fig.2 The CFOA (a) Symbolic representation (b) CMOS CFOA derived from

$$\begin{bmatrix} I_1 \\ I_2 \end{bmatrix} = k(2V_C - V_{thn} - |V_{thp}|)\begin{bmatrix} 1 & -1 \\ -1 & 1 \end{bmatrix}\begin{bmatrix} V_1 \\ V_2 \end{bmatrix} \quad (1)$$

Above equation represents a electronically controllable floating resistance, which value is given as:

$$R_{eq} = \frac{1}{k(2V_C - V_{thn} - |V_{thp}|)} \quad (2)$$

whose value can be changed through the applied control voltage V_C.

The simplified symbol of the CMOS current-feedback operational amplifier (CFOA) is given in Fig.2(a). The internal architecture of the CMOS CFOA is shown in Fig.2(b). The parameters of all the transistors have been taken to be the same as given in [12]. The CMOS CFOA is operated at ±1.5V DC power supply voltage. The CFOA is appertaining to the following terminal equations.

$$V_X = V_Y \quad (3)$$

$$V_W = V_Z \quad (4)$$

$$I_Z = I_X \quad (5)$$

$$I_Y = 0 \quad (6)$$

The circuit of the proposed electronically controllable band pass filter is shown in Fig.3. From the mathematical analysis of the band pass filter of Fig.3, the system function of bandpass filter can be represented by:

$$\frac{V_0}{V_{in}} = \frac{s\left(\frac{1}{R_0C_1}\right)}{s^2 + s\left(\frac{1}{R_0C}\right) + \frac{1}{C_1C_2R_1R_2}} \quad (7)$$

From equ. (7) the filter parameters, namely, the center frequency and bandwidth of the filter can be expressed as:

$$H_0 = 1; \omega_0 = \frac{1}{\sqrt{C_1C_2R_1R_2}} \quad (8)$$

$$BW = \frac{1}{R_0C_1} \quad (9)$$

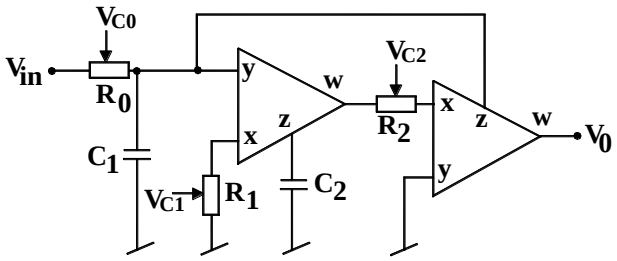


Fig.3 Realisation of a variable-bandwidth/varriable-center frequency band pass filter using the new VCFPR shown in Fig.1

If all the three passive resistors of the band pass filter (BPF) shown in Fig.3 are replaced by the electronically controllable CMOS VCFPRs of the type of Fig.1, from equation (8), the parameter (w_0) of the filter can be expressed as:

$$\omega_0 = \frac{\sqrt{k(2V_{C1} - V_{thn} - |V_{thp}|)k(2V_{C2} - V_{thn} - |V_{thp}|)}}{\sqrt{C_1C_2}} \quad (10)$$

By assuming $V_{C1} = V_{C2} = V_C$ the equ. (10) can be re-written as:

$$\omega_0 = \frac{k(2V_C - V_{thn} - |V_{thp}|)}{\sqrt{C_1C_2}}$$
$$f_0 = \frac{k(2V_C - V_{thn} - |V_{thp}|)}{2\pi\sqrt{C_1C_2}} \quad (11)$$

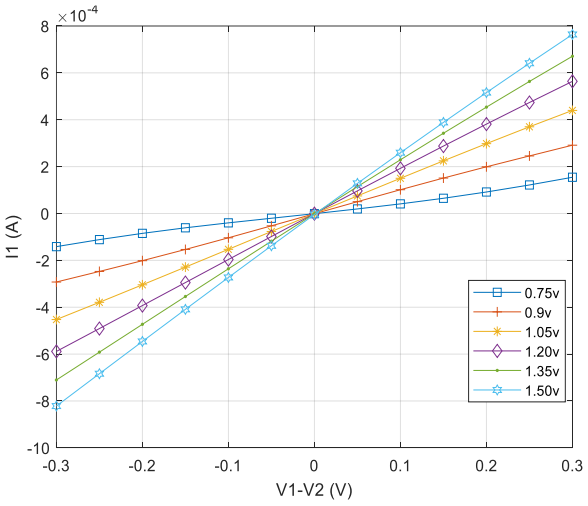
From equ. (11) it may be observed that the parameter (w_0) is electronically controllable and varies linearly with the control voltage V_C. Also, from equation (9), band-width (BW) of the filter can be expressed as:

$$BW = \frac{1}{R_0C_1} = \frac{k(2V_{C0} - V_{thn} - |V_{thp}|)}{C_1} \quad (12)$$

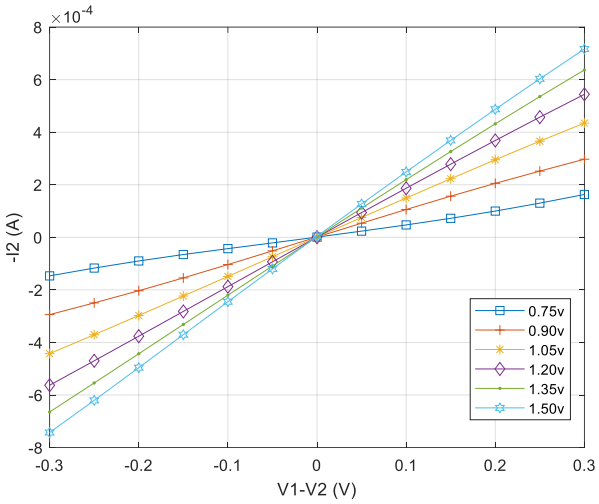
From equ. (12) it is confirmed that the band-width of the proposed bandpass filter is also electronically controllable linearly by the control voltage V_{C0}.

3. SIMULATION RESULTS

To confirm the nature of voltage control floating positive resistance (VCFPR) of Fig.1, this circuit is simulated on 0.18µm TSMC CMOS parameters by catching the parameters of all the MOSFETs same as in [8]. The DC analysis of the VCFPR is shown in Fig.4, from which it may be observed that the resistance value of the VCFPR changes from 2.57KΩ to 0.445 KΩ when control voltage is changes from 750mV to 1500mV at the step of 0.15V. The veracity of the electronic tunability of ω_0 and BW of the BPF was checked by the SPICE simulation of the circuit of Fig.3 using CMOS CFOA shown in Fig.2 biased with ±1.5V, with component values taken as R_1=1kΩ, R_2=2.103 kΩ, C_1=C_2= 0.01 µF. By altering the control voltage V_{C0} from 750mV to 1500mV at a step of 0.15V, the bandwidth of the circuit was changes from 7.493 kHz to 44.468 kHz which is shown in Fig.5. In the same circuit, with the VCFPR of Fig.1 was then employed in place of resistance R_1 and R_2 with equal control voltages V_{C1} = V_{C2} = V_C the center frequency was found to be variable from 6.20 kHz to 42.17 kHz by altering the control voltage from 750mV to 1500mV, which is given in Fig.6, for different values of the controlling voltage V_C, from where the corresponding changes in the bandwidth can be observed.



(a)



(b)

Fig.4 DC analysis of Fig.1(a) Input port current (I_1) Vs. differential input (b) output port current (-I_1) Vs. differential input [1]

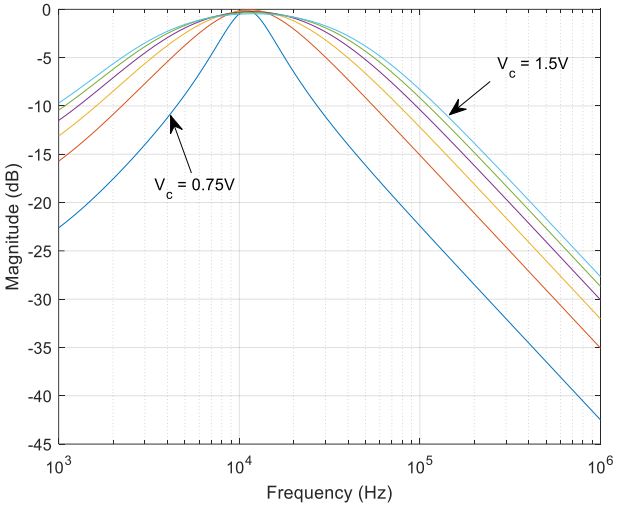


Fig.5: Frequency response of the variable bandwith bandpass filter of Fig.3

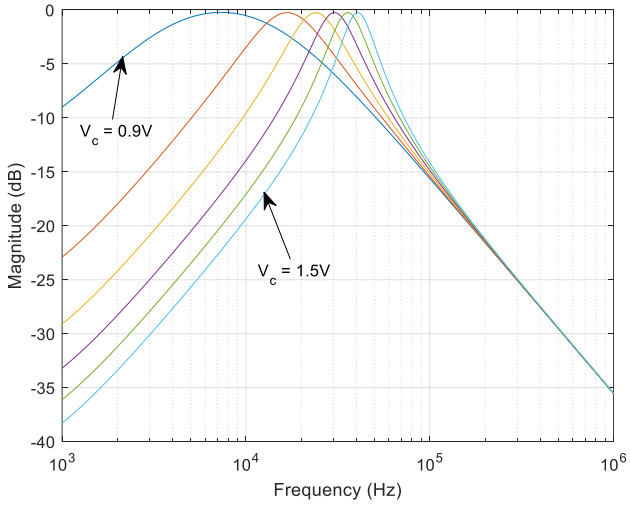


Fig.6: Frequency response of the variable-centre-

frequency band pass filter realised from the circuit of Fig.3

4. CONCLUSION

In this communication a CMOS floating electronically controllable positive resistance configuration has been shown to work out the value of resistance in the range of 2.57 kΩ to 0.411 kΩ which was controlled by the controlling voltage V_C being changed from 0.75V to 1.5V. This circuit exhibits that the input is linear over the range -300mV to +300mV. This circuit is then used to realize an electronically controllable bandwidth and center frequency band pass filter. The workability of which has been validated by CADENCE SPICE simulations using 180nm TSMC CMOS technology parameters.

REFERENCE

[1] P.V Anandmohan, Generation of OTA-C Filter structures from Active RC filter structure, *IEEE transaction on circuits and systems*, 37(5), 1990 656-660.

[2] E. Sánchez-Sinencio and J. Silva-Martínez, CMOS transconductance amplifiers, architectures and active filters: a tutorial, *IEE Proceedings - Circuits, Devices and Systems*, 147(1), 2000, 3-12.

[3] Ali Namdari, Mehdi Dolatshahi, A new ultra low-power, universal OTA-C filter in subthreshold region using bulk-drive technique, *AEU-Internatioanl Journal of Electronics and Communications*, 82, 2017, 458-486.

[4] L. Ramejani, An adjustable bandwidth analog CMOS Gm-C filter, *10th IEEE International Conference on Electronics, Circuits and Systems,* Sharjah, 2003, 420-422.

[5] H. P. Chen, Yi-Zhen Liao and Wen-Ta Lee, Tunable mixed-mode OTA-C universal filter, *Analog Integr Circ Sig Process*, 58, 2009, 135–141.

[6] V. K. Singh, A. K. Singh, D. R. Bhaskar and R. Senani, Novel mixed-mode universal biquad configuration, *IEICE Electronics Express*, 2(22), 2005, 548–553.

[7] D. R. Bhaskar, A. K. Singh, R. K. Sharma, and R. Senani, New OTA-C universal current-mode/trans-admittance biquads, *IEICE Electronics Express*, 2(1), 2005, 8–13.

[8] L.T. Bruton, Electronically tunable analog active filters, *IEEE Transactions on Circuit Theory*, 19(3), 1972, 299-301.

[9] A. Fabre, O. Saaid, F. Wiest and C. Boucheron, "High Frequency Applications Based on a New Current Controlled Conveyor," *IEEE Transactions on Circuits Systems-I*, 43(2), 1996, 82-91.

[10] R. Senani, D.R.Bhaskar, A.K.Singh Second generation controlled current conveyor (CCCII) and their application applicaions Chater-9 of the Current conveyors: variants, applications and hardware implementations, *Springer International puclishing Switzerland*, pp-255-303, 2015.

[11] R. Senani, M. Rai and A. K. Singh, New CMOS linear voltage-controlled floating positive and negative resistances, *Analog Integr. Circuits Signal Process*, 112, 2022, 197-206.

[12] A. Raj, D.R. Bhaskar, P. Kumar, Novel architecture of four quadrant analog multiplier/divider circuit employing single CFOA, *Analog Integrated Circuits and Signal Processing*, 108(6), 2021, 689-701.